Remarks

Applicants respond hereby to the office action mailed from Patent office on May 19, 2005. Applicants thank the Examiner for the Allowance of claims 13-20, and the indication of the allowability of claims 5-9. Applicants have amended the specification at page 6, and have removed the erroneous reference to 15C, and respectfully request withdrawal of the drawing objection set forth at paragraph 2 of the outstanding office action.

103 Rejections

Claims 1-4 under 35 USC 103(a) as unpatentable over US Patent No. 5,550,872, to Liberti combined with applicants' admitted prior art, and US Patent No. 6,567,467 to Wu. In particular, the Examiner asserts that Liberti discloses apparatus for improving reception in a receiver with N antennae (Fig. 2, element 8), where N is greater than 2, including N first receiver chips (Fig. 2, element 218), associated with one of the antennae (Element 108), a digital combiner (elements 218 and 221 connected to first receiver chip (218), with N-1 first buffer memories (element 218, 318), N_1 second buffer memories (222, 406) and a clock synchronizing module 216, col. 6, lines 48-54, where each buffer memory generates an output (222), col. 10, lines 63-67, etc., and that it would have been obvious to combine the admitted prior art with Liberti ' Branch DSP processor (element 218), and it would have been obvious to the skilled artisan to combine the combination with Wu.

Applicants respectfully disagree.

That is, applicants independent claims, such as claim 1, recite apparatus for improving reception in a receiver having N antennae, where N is an integer number with a value equal to or greater than 2. The apparatus includes N first receiver chips each associated with one of said antennae, each chip comprising a front-end section, equalizer, and a back-end section; a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing module, with each buffer memory generating an output signal; a common bus coupled to said first receiver chips and said digital combiner circuit; said clock synchronizing module capable of generating a delay signal and aligning said output signal of each buffer memory based on a common clock; said digital combiner circuit capable of generating a combined output signal; and a single

second receiver chip for receiving said combined output signal of said digital combiner circuit, said second receiver chip comprising a front-end section, equalizer and a back-end section.

Liberti discloses a FFT method and system for ratio combining; Liberti does not disclose a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing circuit as required in each of applicants' independent claims. Hence, combing Liberti, applicants prior art and Wu, assuming arguendo that there would be some reason under the law for making the triple combination, would still not realize applicants inventions as set forth in independent claim 1. Applicants, therefore, respectfully request withdrawal of the rejection of claim 1.

Moreover, because claims 2-4 depend from claim 1, applicants respectfully assert that claims 2-4 are patentable for at least the same reasons set forth for the patentability of claim 1, and request withdrawal of the 103 (a) rejections of claims 2-4.

Claim 10 was rejected under 35 USC 103(a) as unpatentable over Liberti, applicants admitted prior art and Wu, like claim 1, and further in view of US Patent No. 6,438,570 to Miller.

Applicants respectfully disagree.

Because claim 10 depends from claim 1, and Liberti fails to disclose a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing circuit as required in each of applicants' independent claims. So even making the by-four combination would still not realize a digital combiner circuit of claim 1, and therefore the combined art will still not realize an invention as set forth in applicants claim 10. Hence, applicants respectfully request that the rejection of claim 10 under 103(a) in view of Liberti, applicants admitted art, Wu and Miller be withdrawn.

Claim 11 was rejected under 35 USC 103(a) as unpatentable over Liberti, applicants admitted prior art and Wu, like claim 1, and further in view of US Patent No. 6,4,141,609 to Moss.

Applicants respectfully disagree.

Because claim 11 depends from claim 1, and Liberti fails to disclose a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing circuit as required in each of applicants' independent claims. So even making the by-four combination would still not realize a digital combiner circuit of claim 1, and therefore the combined art will still not realize an invention as set forth in applicants claim 11. Hence, applicants respectfully request that the rejection of claim 10 under 103(a) in view of Liberti, applicants admitted art, Wu and Moss be withdrawn.

Claim 12 was rejected under 35 USC 103(a) as unpatentable over Liberti, applicants admitted prior art and Wu, like claim 1, and further in view of US Patent No. 4,720,812 to Kao.

Applicants respectfully disagree.

Because claim 12 depends from claim 1, and Liberti fails to disclose a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing circuit as required in each of applicants' independent claims. So even making the by-four combination would still not realize a digital combiner circuit of claim 1, and therefore the combined art will still not realize an invention as set forth in applicants claim 12. Hence, applicants respectfully request that the rejection of claim 10 under 103(a) in view of Liberti, applicants admitted art, Wu and Kao be withdrawn.

Claim 21 was rejected under 103(a) over Liberti in view of US Patent No. 5568443 to Dixon, where the Examiner asserts that Liberti's elements 221 and 218 teach applicants claimed combiner circuit.

Applicants respectfully disagree.

Claim 21 claims, like independent claim 1, a combiner circuit. Liberti elements 221 and 218 does not realize a combiner circuit as claimed, so applicants respectfully assert that claim 21 is not obvious under 103(a) by the Liberti/Dixon combination, and further request withdrawal of the claim 21 rejection.

Allowance and passage to issue of this application is respectfully requested.

Respectfully submitted,

By _____

John F. Vodopia, Reg. 36,299
Attorney for Applicants (914) 333-9627

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited this date with the United States Postal Service as first-class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

On 08/19/2005
(Mailing Date)

By _____
(Signature)